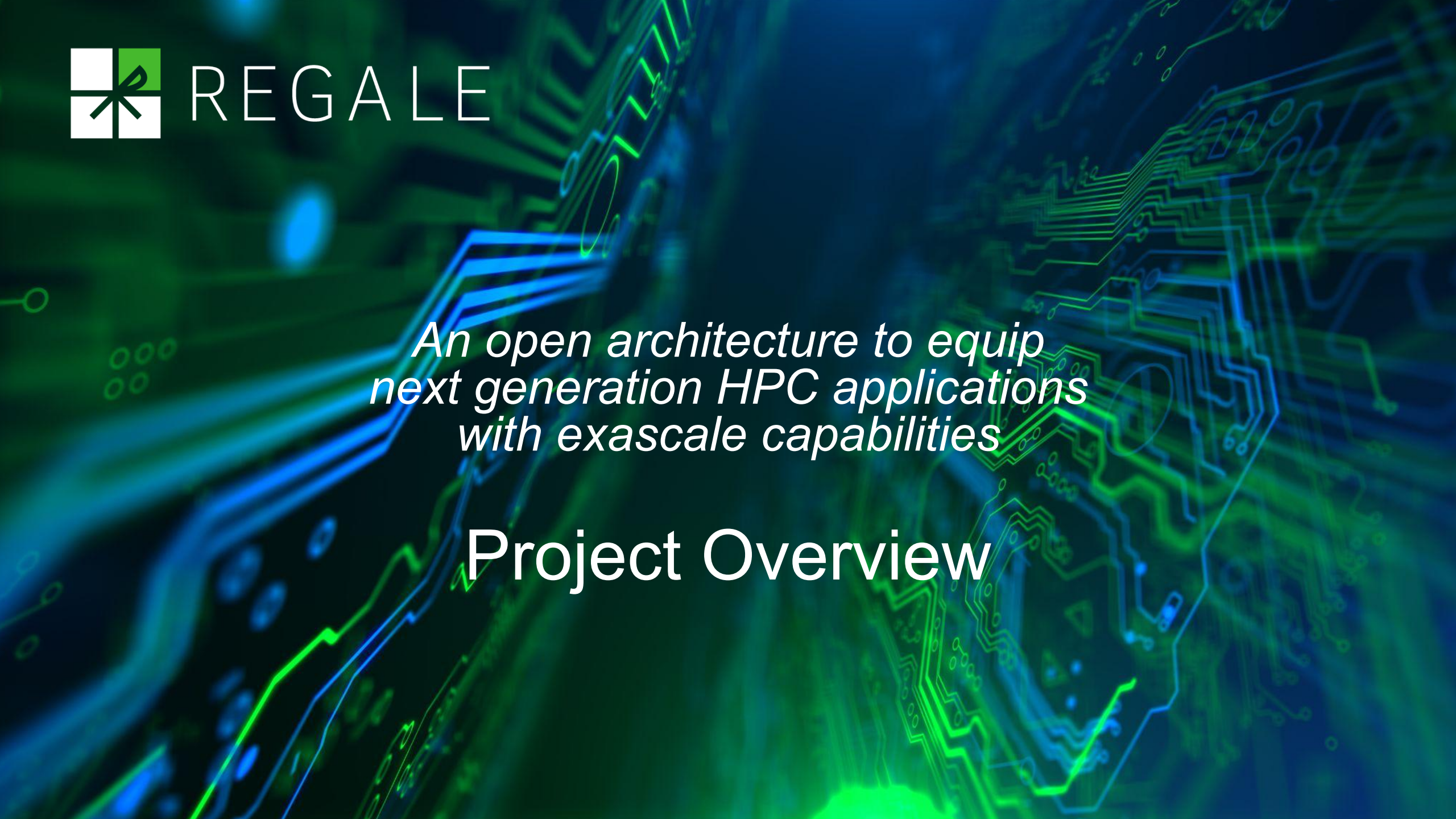


An open architecture to equip next generation HPC applications with exascale capabilities

Project Overview

REGALE

Project info

Project info

Call: H2020-JTI-EuroHPC-2019-1

Funding scheme: EuroHPC-IA

Start date: 1 April 2021 **End date:** 31 March 2024

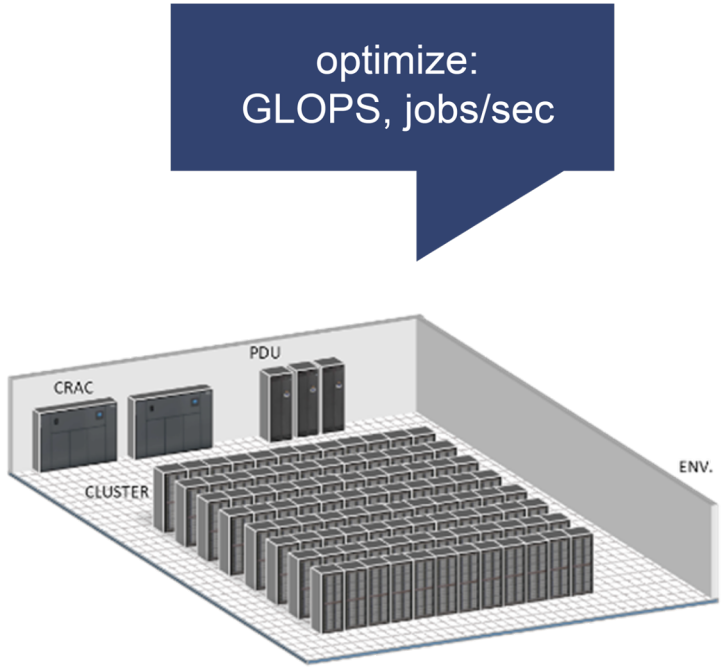
Consortium:

REGALE

REGALE motivation

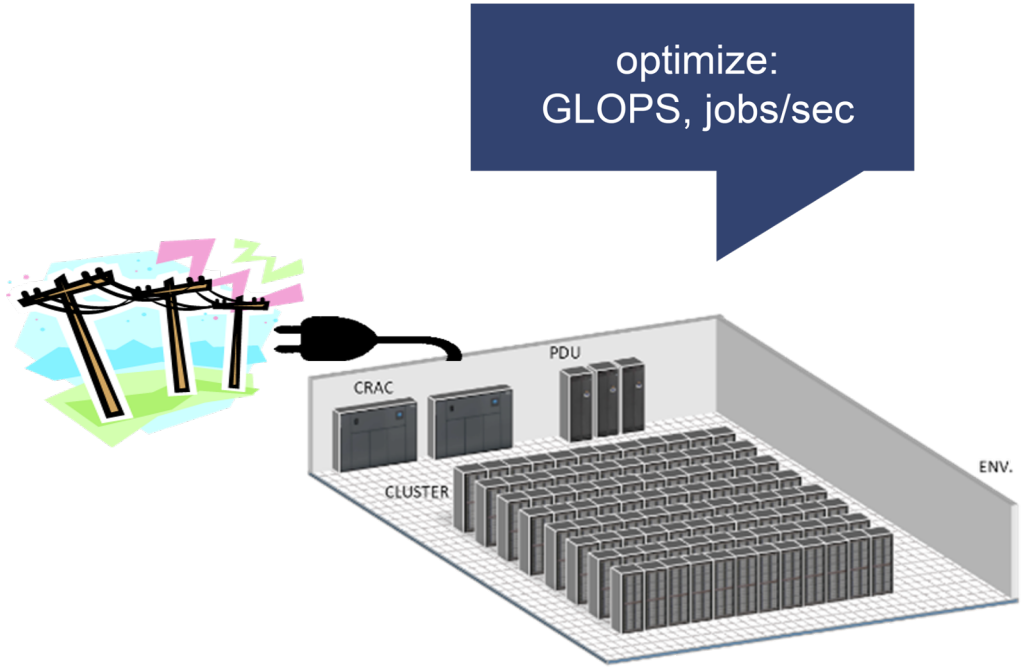
REGALE motivation: system side

Traditional supercomputing is about performance and throughput



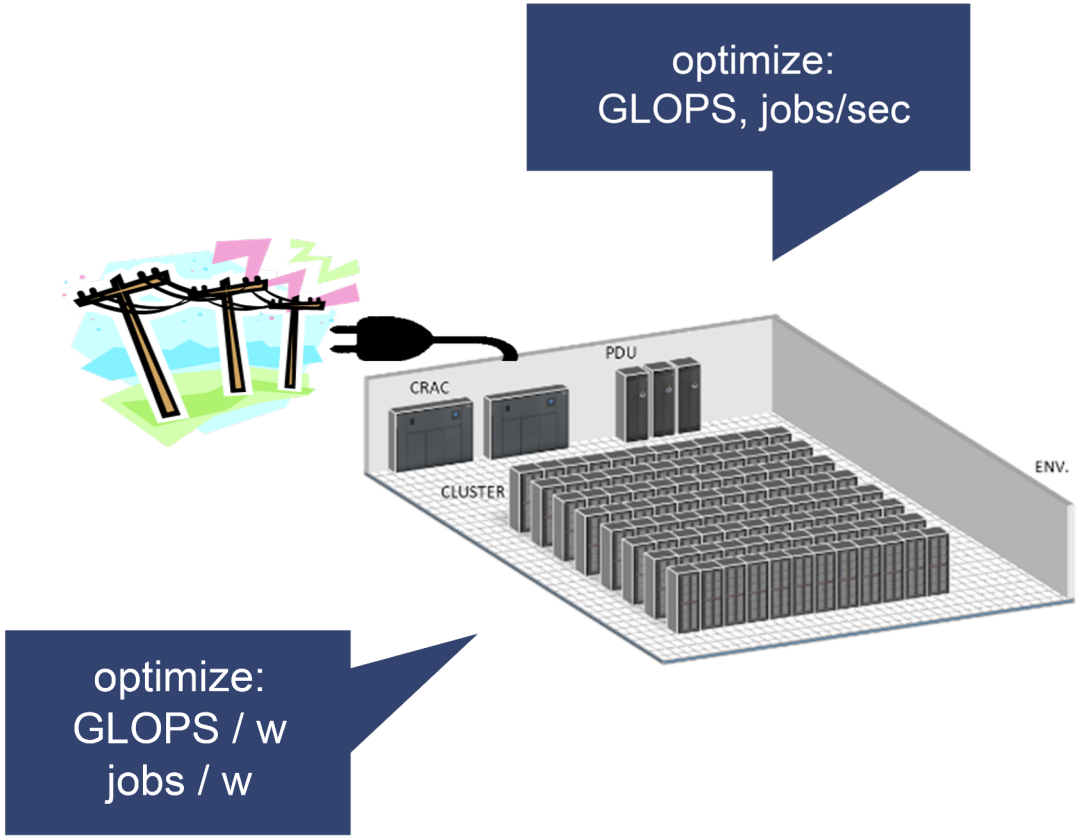
REGALE motivation: system side

But modern supercomputers are hungry energy consumers…



REGALE motivation: system side

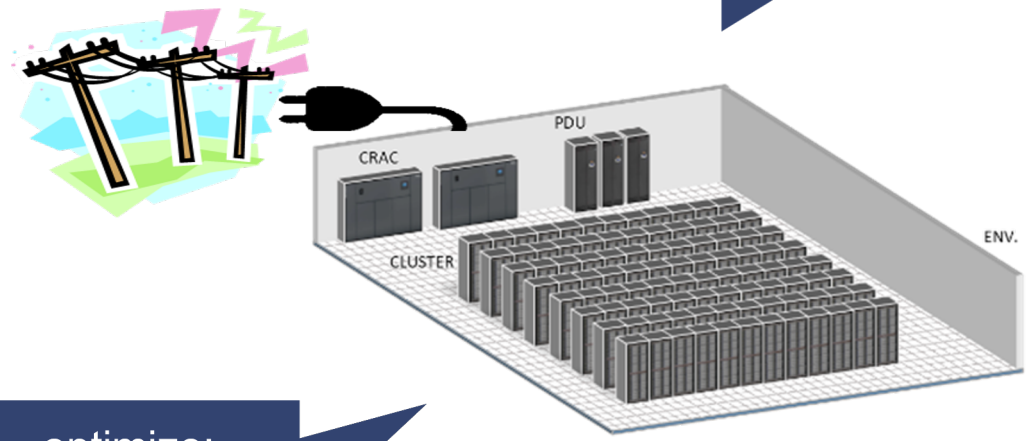
… they need to save energy…

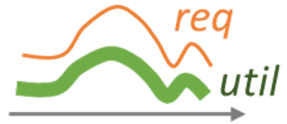


REGALE motivation: system side

… and operate under power constraints

optimize:
GLOPS, jobs/sec



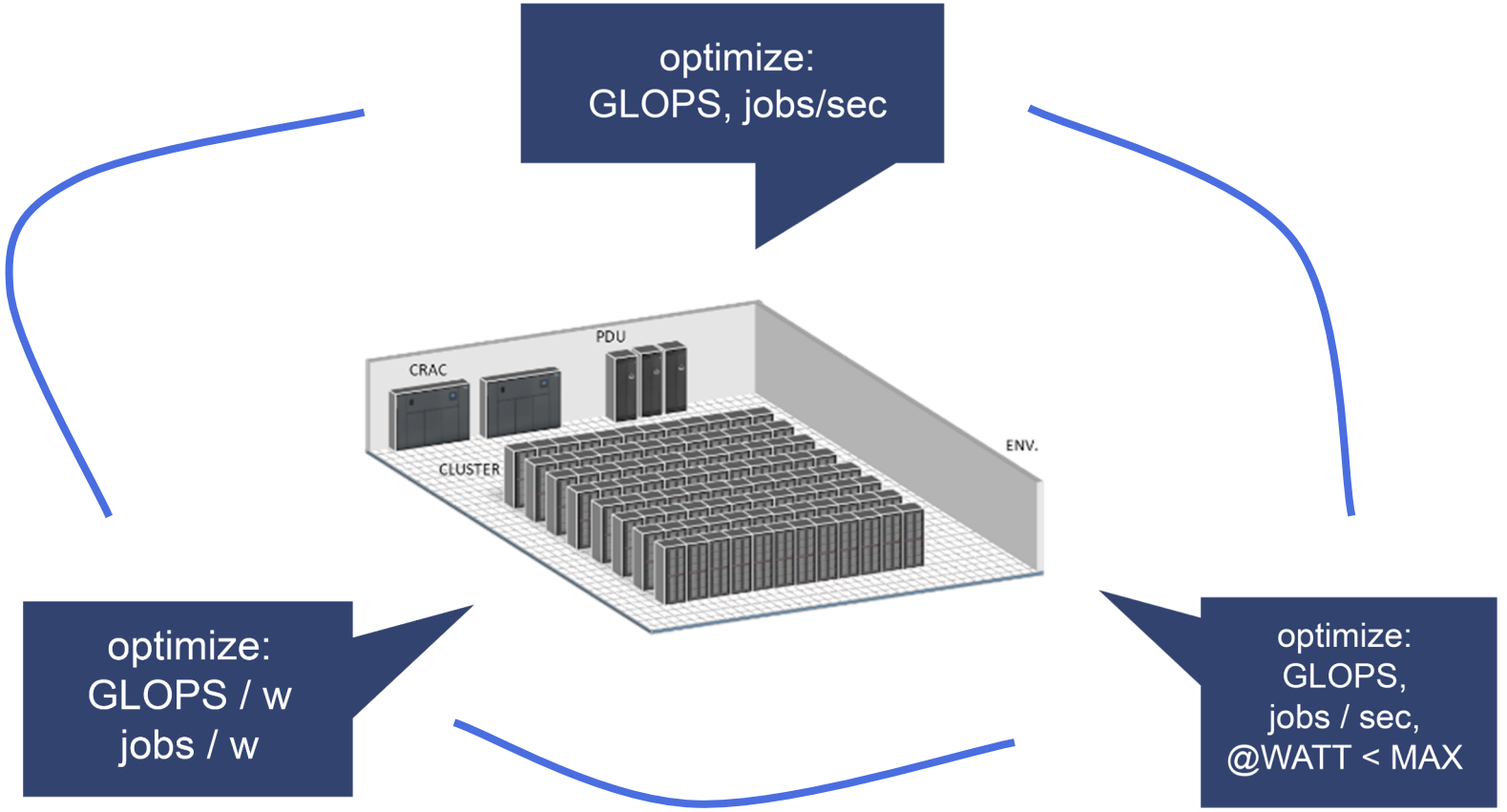


optimize:
GLOPS / w
jobs / w

optimize:
GLOPS,
jobs / sec,
@WATT < MAX

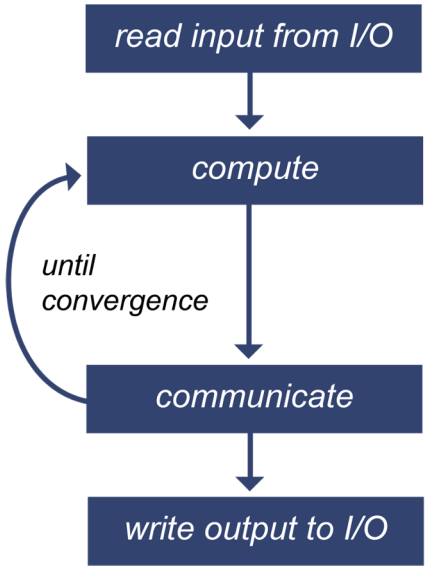
REGALE motivation: system side

New modes of operation for the supercomputer



REGALE motivation: application side

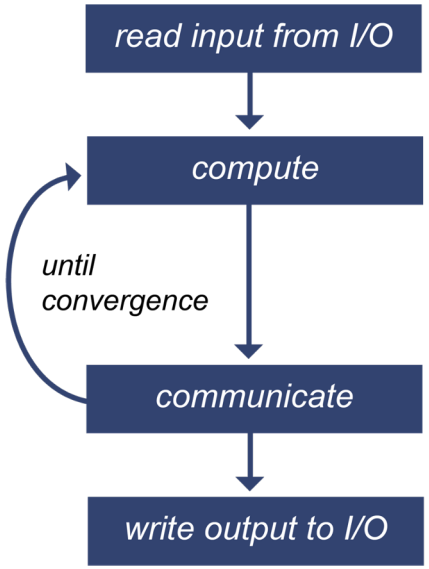
Traditional HPC applications have a rather simple structure

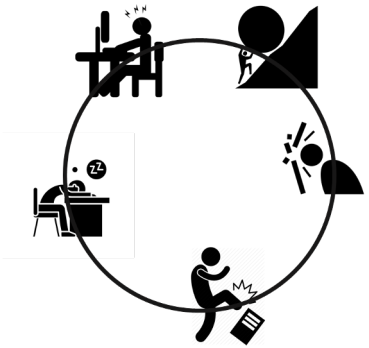


traditional HPC application

REGALE motivation: application side

… and leave the programming and optimization complexity to the programmer …

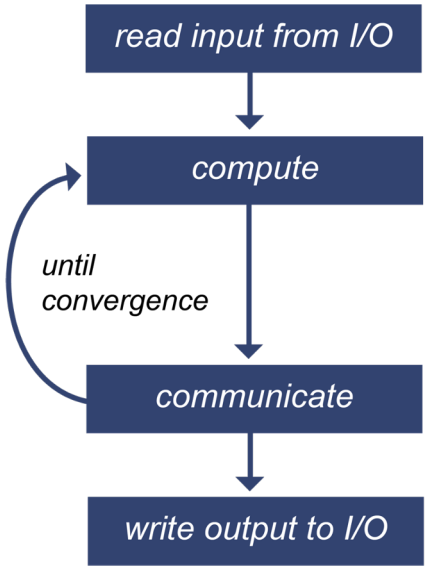




traditional HPC application

REGALE motivation: application side

… requiring extraordinary skills (domain expertise + parallel programming + performance engineering)

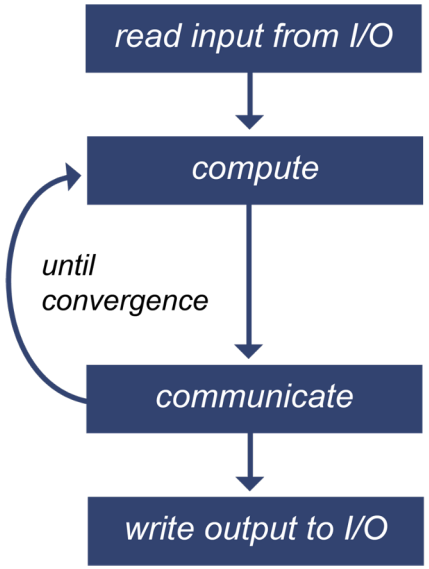


traditional HPC application

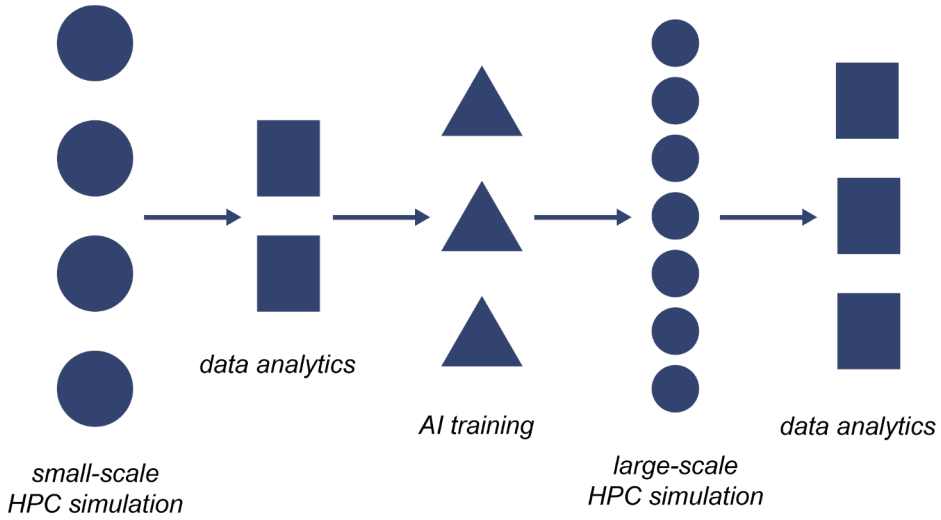
HPC programmer

REGALE motivation: application side

… can we follow the same approach for the highly complex next generation of HPC applications?



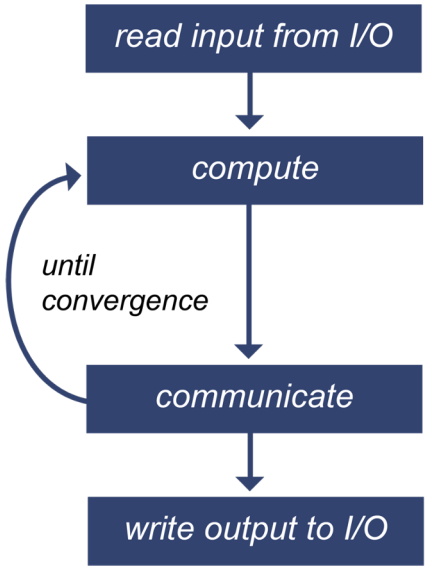
traditional HPC application



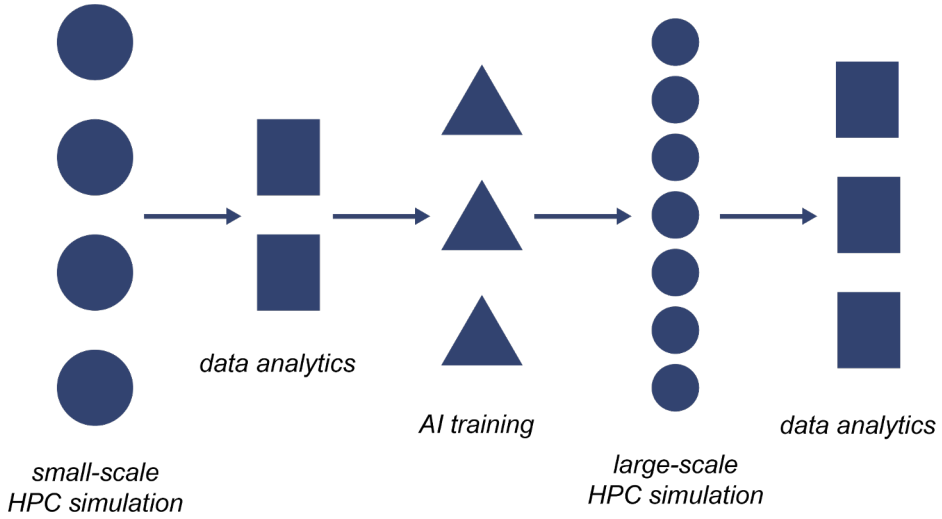
next generation HPC application
(workflow)

REGALE motivation: application side

… special tools (workflow engines) need to make the lives of programmers easier



traditional HPC application



next generation HPC application
(workflow)

REGALE

Project vision and objectives

REGALE vision

To pave the way of next generation HPC applications to energy efficient exascale systems

Sought by:

- The definition on an **open architecture**
- The instantiation of a **prototype system** integrating EU technology
- The incorporation of **sophistication** from top academic experts
- The evolution of five **key pilots**

Project strategic objectives

Effective utilization of resources.

- Improved application **performance**.
- Increased system **throughput**.
- Minimization of performance degradation under the operation with **power constraints**.
- Decreased **energy to solution**.

Broad applicability.

- openness
- platform independence
- scalability
- modularity
- extensibility
- simplicity

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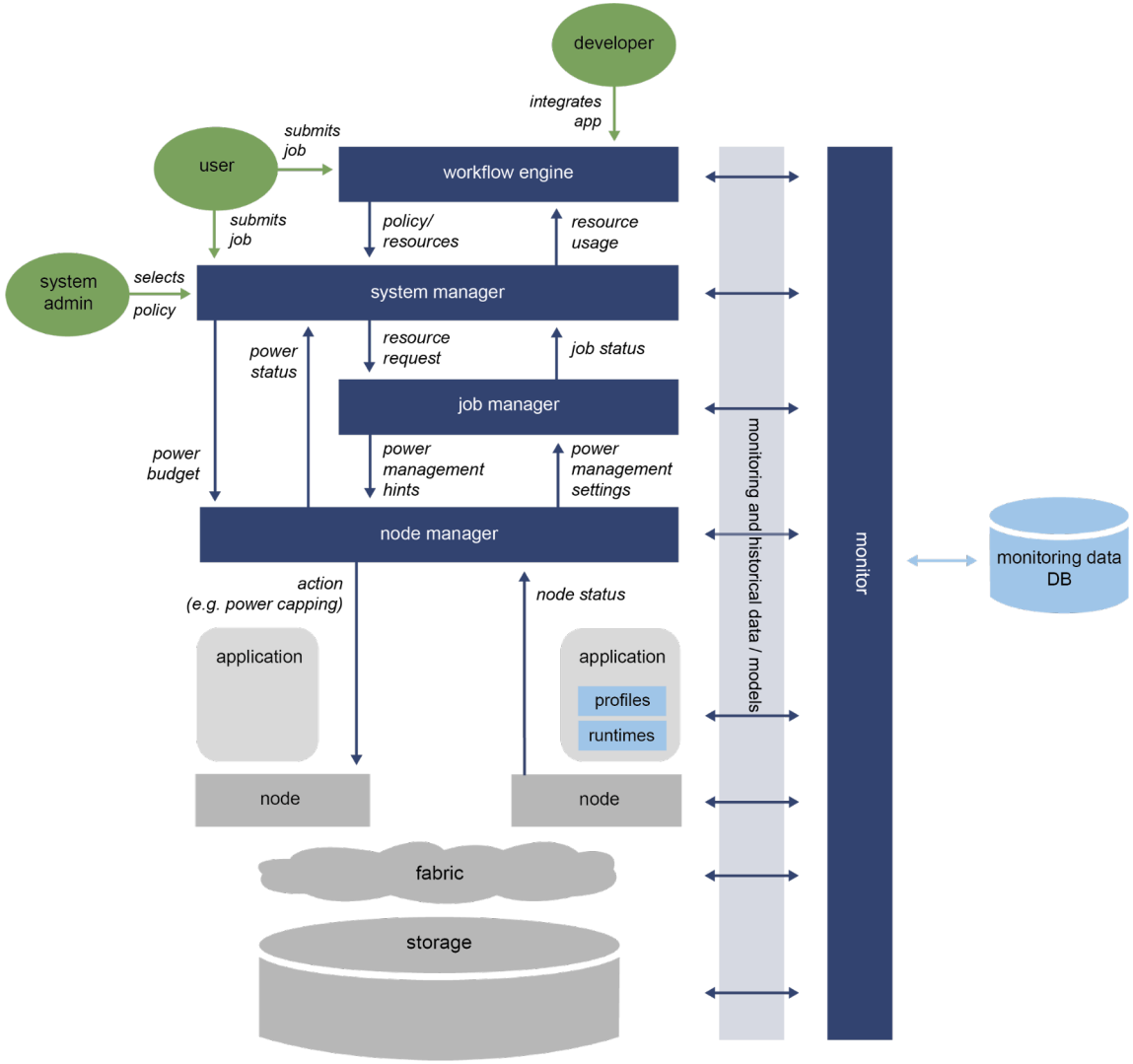
Approach

Regale technical approach

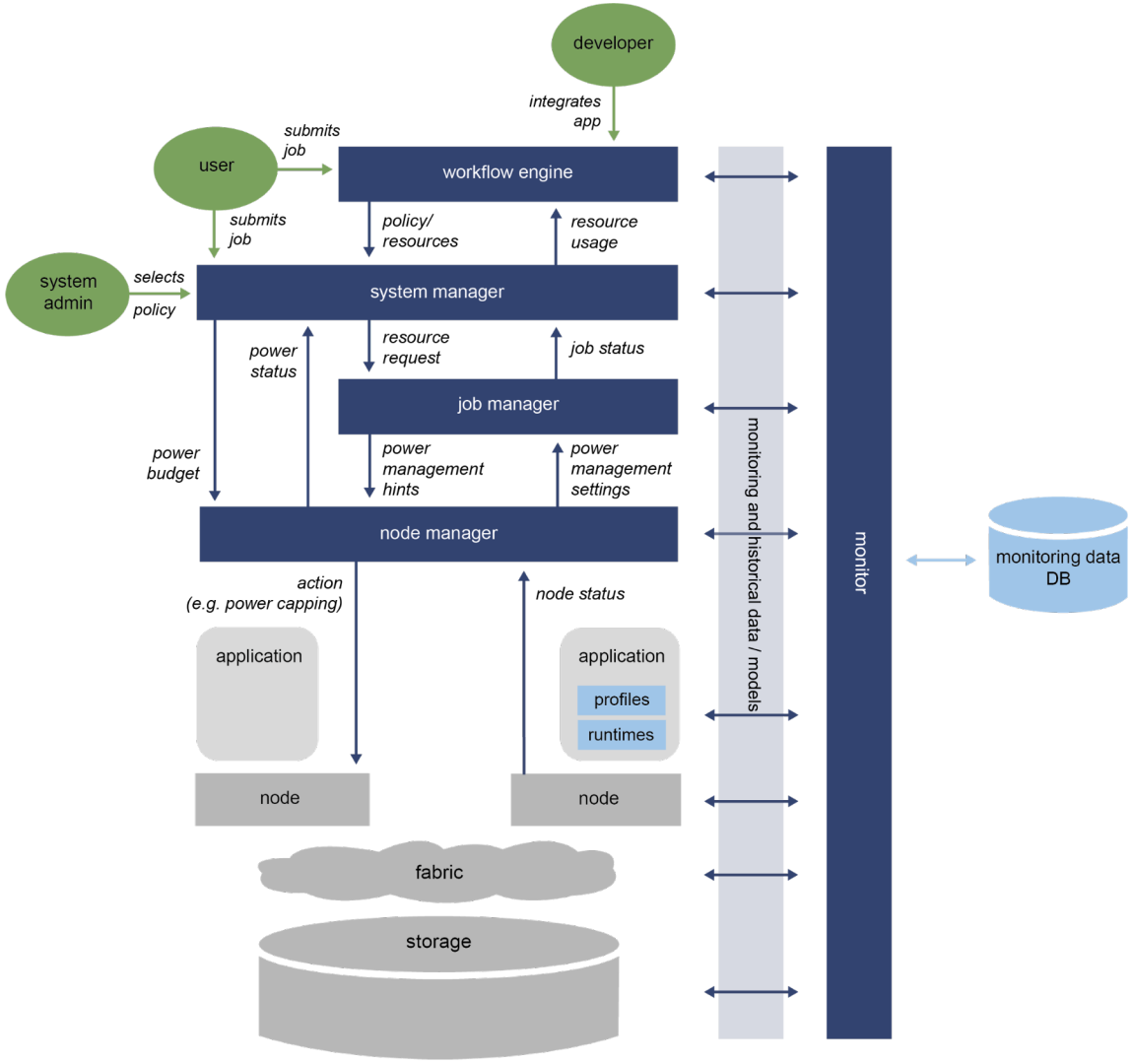
Define an architecture and implement an instantiation that:

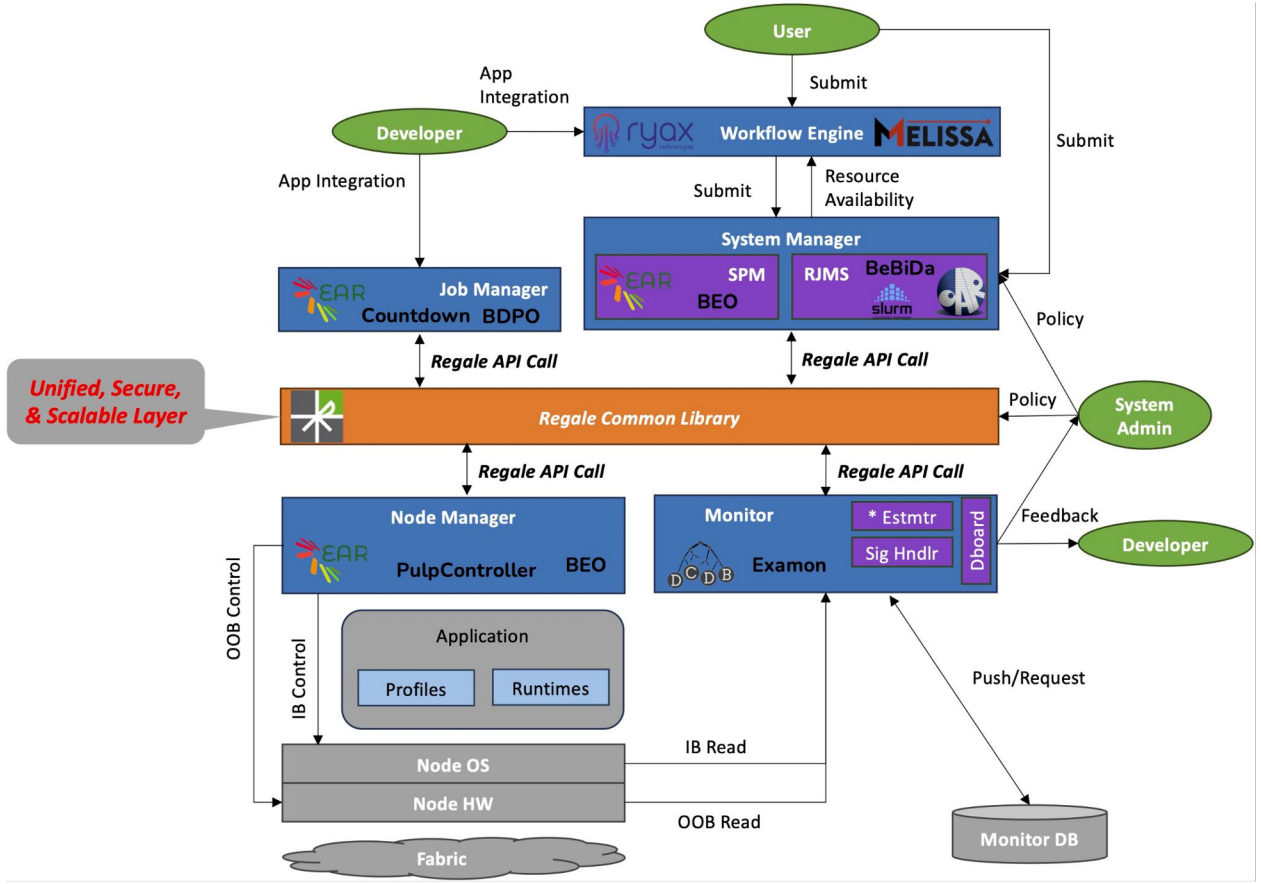
- Switches between different **optimization targets** (performance, energy, power)
- Adapts to **application phases** for effective power capping
- **Co-schedules** applications for increased performance
- Exploits **job moldability** for increased energy efficiency

REGALE architecture



REGALE architecture



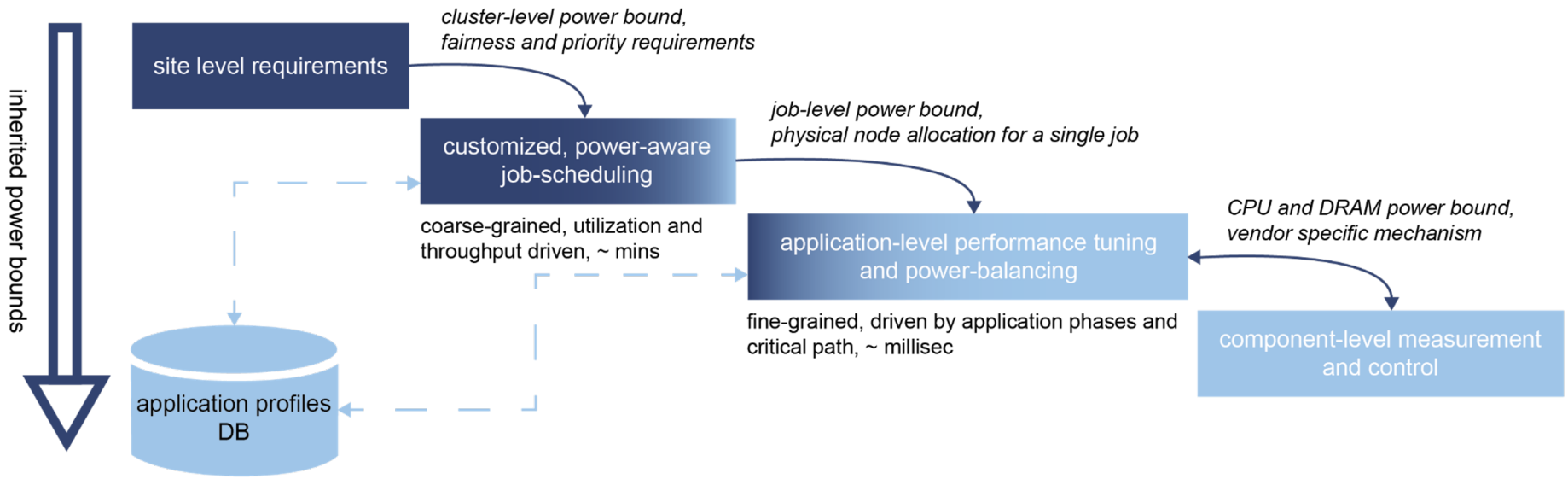


Maximizing the impact

A path to standardization and / or homogenization

A strong connection with the HPC Powerstack: https://powerstack.caps.in.tum.de/

A community of academics, key industrial players and HPC stakeholders



Thank you for your attention!

Contact us!

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Contact us!

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Funding

This project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 956560. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Greece, Germany, France, Spain, Austria, Italy.

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