

PILOTS

REGALE embraces five pilots which act as representatives of the next generation of HPC applications.

We will leverage the unique and diverse characteristics of these data-intensive HPC workflows to co-design the REGALE architecture, continuously evaluate the REGALE prototypes, and adapt the pilots themselves to the REGALE architecture in order to unleash their full potential at extreme scale.

OUR PILOTS ARE:

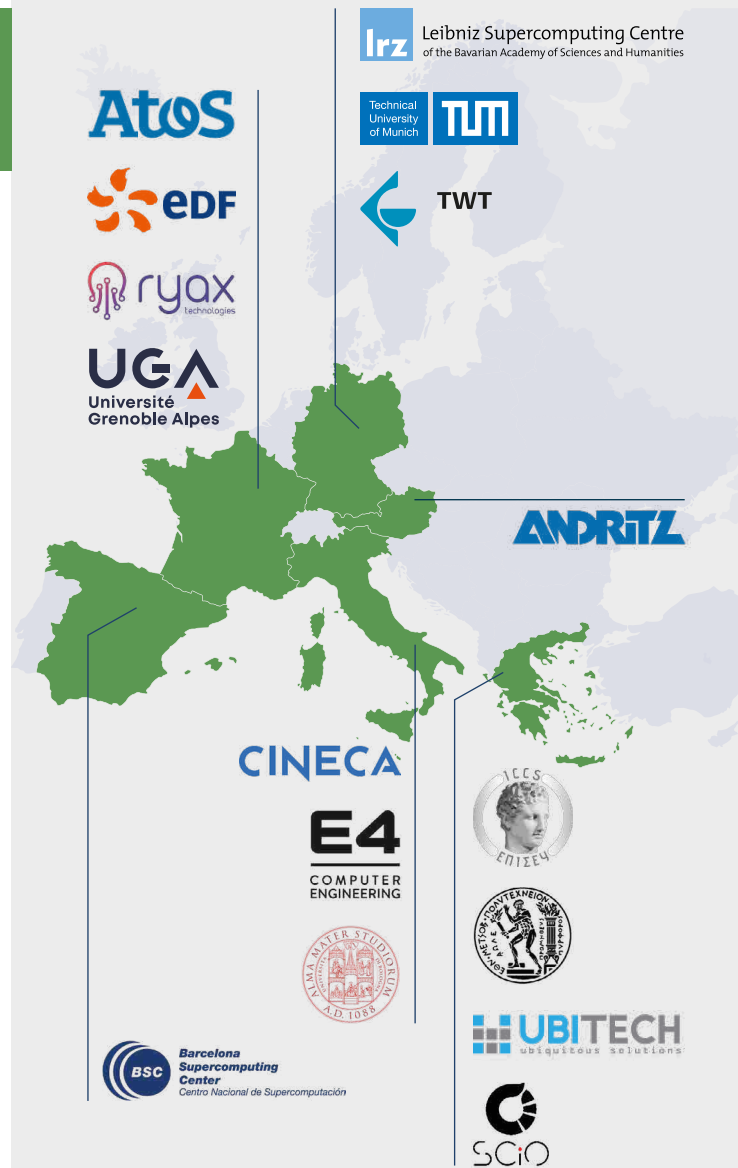
Industrial Scale Unsteady Adjoint-based Shape Optimization of Hydraulic Turbines

In-Transit Workflow for Ubiquitous Sensitivity Analysis and MetaModel Training

Enterprise Risk Assessment with High Performance Data Analytics

Complex geomorphometric models executed over earth observation data for groundwater estimation and management

Design of car bumper made up from carbon reinforced polymers



CONTACT US

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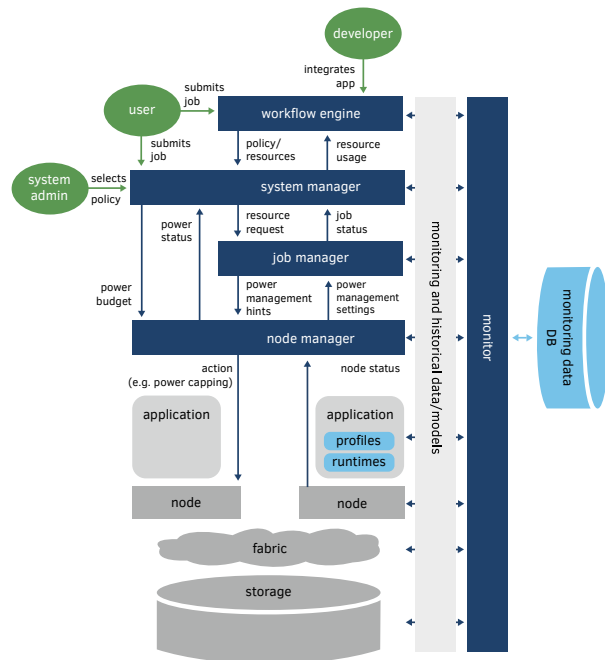
Twitter: [@EuRegale](https://twitter.com/EuRegale)



Open Architecture for
Exascale Supercomputers

EFFICIENT, OPEN & SCALABLE

To pave the way of next generation HPC applications to exascale systems, we define an open architecture, build a prototype system and incorporate in this system appropriate sophistication in order to equip supercomputing systems with the mechanisms and policies for effective resource utilization and execution of complex applications. The open architecture of REGALE integrates together state-of-the-art HPC software modules like MPI and SLURM with European tools like OAR, DCDB, BEO, EAR, Melissa and others that enhance the system's energy efficiency and programmability.



OPEN ARCHITECTURE FOR FUTURE SUPERCOMPUTERS

Supercomputers in the near future will be much more than just larger and more powerful machines than the ones used today. We are approaching exascale systems and with that, some paradigms of HPC will become obsolete.

Future systems will be very heterogeneous and complex on node level. They will leverage very different technologies, such as general-purpose CPUs as well as GPU and FPGA accelerators. For energy efficient computing without significant trade-off on the performance side, applications will have to leverage these technologies dynamically. To achieve this, a new software stack is needed.

REGALE brings together leading supercomputing stakeholders, prestigious academics, top European supercomputing centers and end users from critical target sectors, covering the entire value chain in system software and applications for extreme scale technologies.

The REGALE project aims to build an open and scalable software stack capable of bringing energy efficiency and programmability to tomorrow's HPC exascale systems.

QUICK FACTS

CALL:
H2020-JTI-EuroHPC-2019-1

PROJECT TIMESPAN:
April 2021 – March 2024

CONSORTIUM:
Coordinator: Institute of Communication and Computer Systems

16 Partners
6 European countries

FUNDING



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